I am an RIT alumnus graduated from Microsystem Engineering in 2007. Currently I work at Micron Technology, Boise Idaho. I understand the quality of our RIT grads and proud of being RIT alumni. I am coming to RIT for the campus career fair on Mar 30th. There are two openings that would be very good for Imaging Science grads. They can directly send their resume to me (jzhou@Micron.com) before the career fair so I can schedule some interview on 31st or they can stop by our booth.
Thanks for help!
Jianming
PH.D
Photolithography Engineer
Micron Technology

RET Engineer - BOI24962

As a Reticle Enhancement Technology (RET) Engineer in the Optical Proximity Correction (OPC) area at Micron, you will be responsible for developing process strategies for resolution enhancement techniques, including, but not limited to: OPC, illumination optimization, scatter bar optimization and application, phase shift lithography and custom illuminator design. The scope of these responsibilities include development of current and future R&D reticle strategies, as well as supporting relevant issues in production with reticle solutions. You will also support the design and layout groups with input on design rules to generate robust and manufacturable designs for the process development and production groups. Currently hiring for positions in Boise and San Jose to support Micron's world-wide production fabs.

Qualifications Successful candidates for this position will have:

- 3+ years experience in reticle development in the semiconductor industry, preferably with direct input on data correction from design and layout to improve printability of the process.
- Very strong computer skills, including familiarity with Windows, Linux, UNIX, and some experience with programming languages (Perl/C/C++/TCL/Python).
- Experience with photolithography simulation packages, such as Solid-C, S-Litho, Prolith, etc.
- Strong knowledge in photolithography theory, including optics, diffraction, phase shifting and resist modeling. Proven experience with 248 nm, 193 nm and 193 nm immersion lithography.
- Knowledge of automation tools, like Cadence DF2 and Hercules. (Preferred)
- Experience with software packages developed by any EDA vendor (Synopsys, Mentor Graphics, BRION, etc.), preferably in the areas of rule or model based assist feature design, OPC empirical model creation and lithography simulations.
- Any related experience in layout of data, including knowledge of DRC/LVS methods.
- Demonstration of skills in project management.
- The ability to be highly motivated, goal oriented, and aggressively focus on solving problems both as part of a team and individually.
- Excellent verbal and written communication skills to be effective.
- Proven ability to manage projects effectively to meet deadlines and work independently with minimal supervision.

Education:

M.S. or Ph.D. in engineering or relevant sciences (i.e., Physics, Optics, etc.) is required.

Job: Process Engineer

Primary Location: North America-US-Idaho-Boise

Other Locations: North America-US-California-San Jose

Job Posting: Jan 28, 2011

Unposting Date: Ongoing

Relocation Provided: Yes